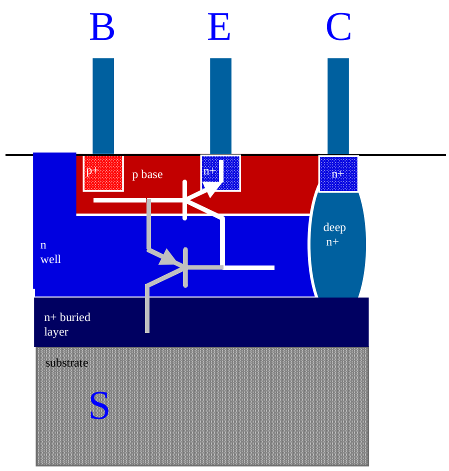
IC-CAP Toolkit for

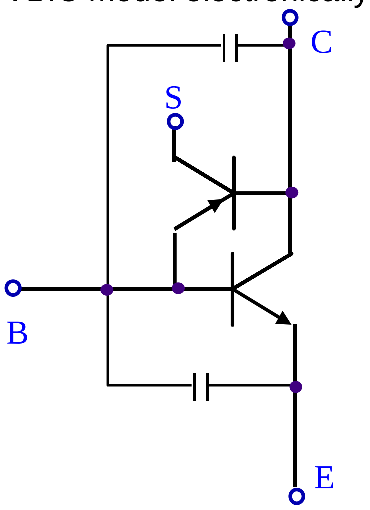
VBIC

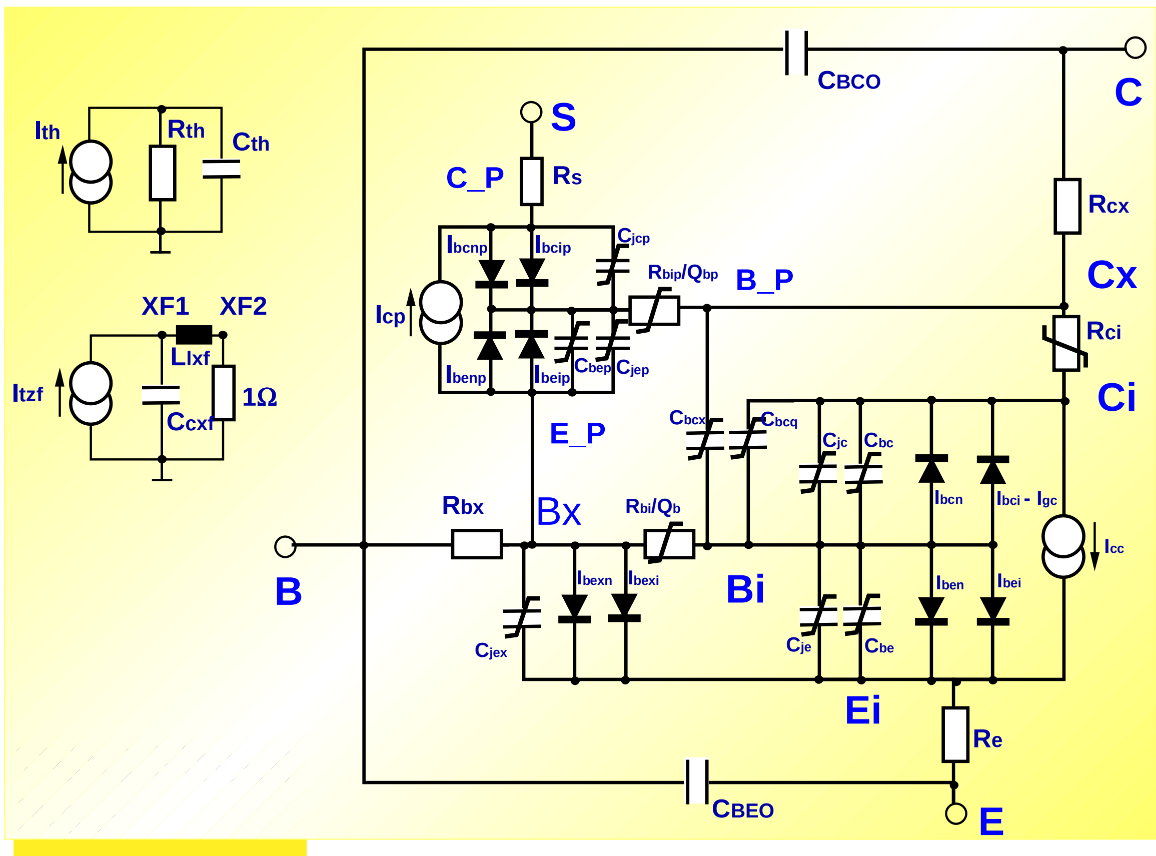
The Vertical Bipolar Inter-Company Bipolar Model

VBIC model physically



VBIC model electronically





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1. Introduction

In 1954, Ebers and Moll have proposed a large signal model for bipolar transistors. This model is still the background of today's bipolar transistor models. It describes the fundamentals of the DC behavior. However, low and high current effects, as well as parasitic resistors and dynamic behavior are not yet covered. Fig.1 depicts the topology of the underlying equivalent schematic.

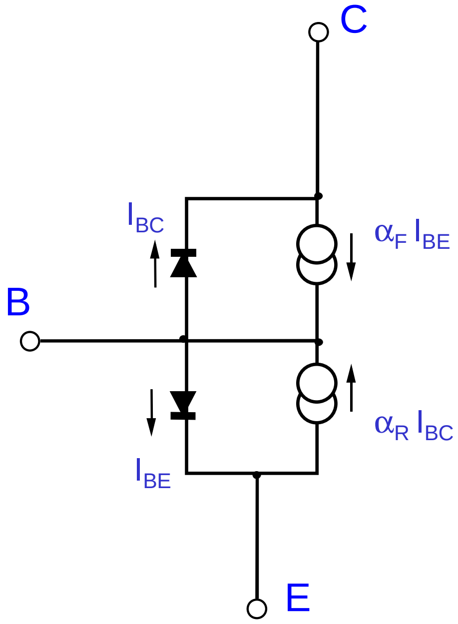

Fig.1: Equivalent schematic for a bipolar transistor after Ebers-Moll.

Based on the schematic of fig.1, an alternate, yet mathematically identical formulation has been introduced. Instead of injection currents, it is based on a transport current. This means, the two current sources of the forward and reverse current are combined into a single current source (Fig. 2). The main difference between both models is the different reference currents. The injection version model is based on both diode currents, while the transport version makes use of the currents ICC and IEC, which give the current ICT.

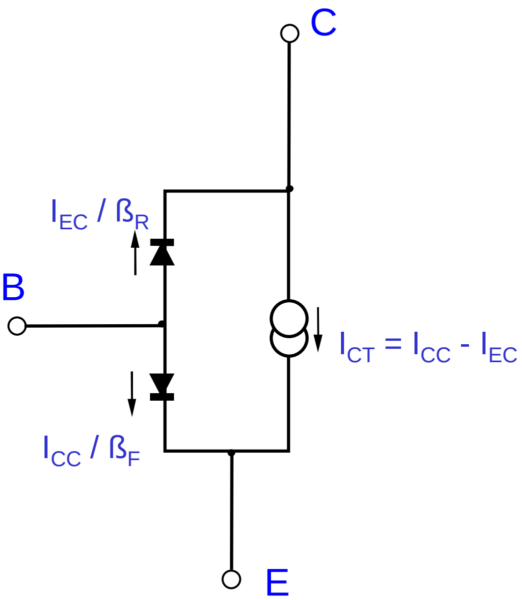

Fig. 2: Hybrid equivalent schematic of the Ebers-Moll model.

This large signal model has been enhanced and improved many times. Pedersen introduced a classification into three Ebers-Moll model versions EM1, EM2 and EM3, see Getreu.

The EM3 model covers already all essential effects, which are then included in the Gummel-Poon model, published in 1970 [see publications]. The important advantage of modeling the bipolar transistor with the Gummel-Poon model is especially the very clear and standardized description of many effects by introducing the "integral charge control relation". Therefore, with the years, the Gummel-Poon (G-P) model has become a standard for the modeling of bipolar transistors.

It should be mentioned, however, that this modeling standard is usually a special version of the G-P model, which has been implemented into the simulation program SPICE of the University of Berkeley UCB, California. In some details, this implementation differs from the original G-P formulation. This is especially true for the Early effect. See e.g. the Agilent ADS implementation which allows to select either the simplified UCB SPICE version, or the original Gummel-Poonm paper model.

For modern transistors with the continuous trend to smaller geometries, second order effects become more and more important. Due to higher integration and the necessity to improve the design yield, the need for more precise simulation results and thus to better models has increased. Many companies have therefore developed in-house models, and in some cases made them public. Such a model is the Philips MEXTRAM model. It was developed in 1986 by de Graaff, Klostermann and Jansen.

Later, in 1995, an US industry consortium has proposed a new bipolar model, called VBIC95. Its goal was to become an accepted standard for today's bipolar transistors. Besides an improved modeling, also including the parasitic PNP transistor of integrated NPN transistors, the VBIC95 is aimed to be as much as possible similar to the standard G-P model. Today, it has changed its name to VBIC.

The following list gives the improvements of the VBIC model compared to the SPICE G-P model:

-> Precise implementation of the Base width modulation
-> Parasitic Substrate transistor
-> Improved Kull model for quasi-saturation
-> Enhanced delay time modeling
-> Approximating a distributed Base region
-> weak avalanche current effects
-> consistent treatment of the additional phase factor for small signal and time domain analysis
-> improved capacitance model
-> self-heating: improved temperature modeling

Since the VBIC is based on the Gummel-Poon model, and since we want to sketch the similarities between both models, we will now recap the details of the standard SPICE G-P model.

A note on PNP transistors:

The VBIC model is focussing by its own name on a vertical bipolar transistor, i.e. per definition to a NPN transistor.

If applied to a PNP transistor, first check its physical structure. Then decide, what kind of sub-circuit you may want to use for the modeling. See /Getreu/.

LATERAL PNP:
has a wide Base, therefore, its 'ß' is low, and as a consequence, its 'ft' is low too.

SUBSTRATE PNP:
has usually the following sequence of layers:

E	p
B	n
C	p of wafer

This means, that its Collector is identical to the substrate, i.e. at negative supply voltage. Such transistors usually feature a bad 'ß'.

VERTICAL PNP (modeling possible using VBIC)

```
 S
| |   E   p   | |
| |   B   n   | |
| |   C   p   | |
|  -----------  |
|        n      |
 ---------------
     p Wafer
```

Its Collector current iC flows vertical, 'ß' is high (because the Base can be made very thin), and as a consequence, its 'ft' is high.