SILVACO

SmartSpice Circuit Simulator

SmartSpice™ Circuit Simulator delivers the highest performance and accuracy required to design complex analog circuits, analyze critical nets, characterize cell libraries, and verify analog mixed-signal designs. SmartSpice is compatible with popular analog design flows and foundry-supplied device models.

- 100% HSPICE™ compatible for netlists, models, analysis features, and results
- Provides the most accurate circuit simulation results for critical analog and nanometer effects
- Offers largest capacity of any true SPICE circuit simulator – up to 400 thousand active devices in 32 bit and 8 million active devices in 64 bit version
- Fastest run-time of any true SPICE circuit simulator and the only SPICE supporting multiple threads for parallel operation
- Robust convergence using multiple solvers and stepping algorithms
- Largest collection of calibrated SPICE models for traditional technologies (Bipolar, CMOS) and emerging technologies (TFT, SOI, HBT, FRAM, etc.)
- Provides open model development environment and extensive analog behavioral capability with Verilog-A option
- Supports Cadence analog flow through OASIS™

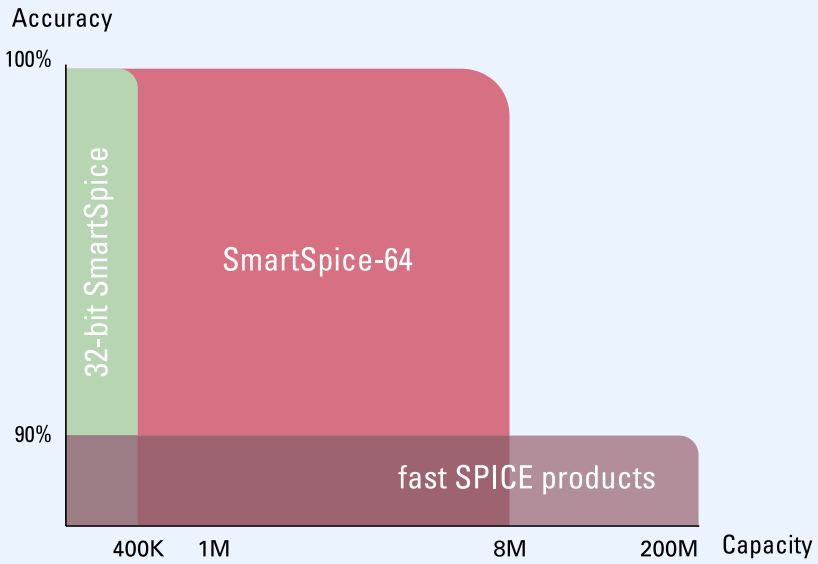
Accuracy: SmartSpice is the most accurate circuit simulator for critical analog and nanometer effects

- Uses Gaussian elimination in an efficient matrix-based on the original Berkeley 3C1 solver
- Includes multiple improved solvers that enhance the classic Newton-Raphson algorithm for the iterative solving of non-linear equations
- Verifies and validates Berkeley physics-based model parameters at run-time for continuity, linearity, and valid parameter range
- Detects inconsistencies in poorly-extracted foundry models and prevents these errors from degrading the final product performance and accuracy
- The simulator of choice at foundries that focus on analog and mixed-signal process accuracy
- Offers a full set of options for controlling speed accuracy of simulations

Capacity: SmartSpice simulates more active devices than any other analog circuit simulator

- Simulates circuits with more than 400K active devices (limited by addressable memory)
- SmartSpice-64 supports simulation of an unprecedented 8 million active devices with full SPICE accuracy on 64-bit workstations

SmartSpice-64 simulates up to 8 million active devices with true SPICE accuracy.



Speed: SmartSpice runs faster than other true SPICE simulators

- Simulates at 2 to 4 times the raw speed of other SPICE products
- Supports multiple parallel 32/64 bit CPUs for near-logarithmic multi-threaded operation

Convergence: SmartSpice selects the right solver for optimal convergence integrity, speed, and stability

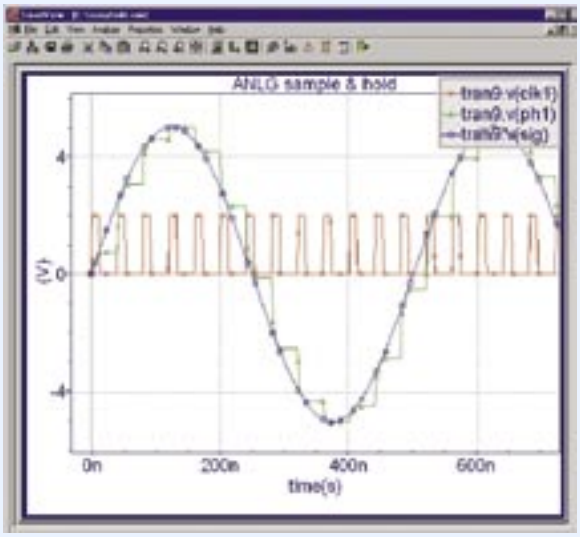
- Surveys initial conditions and iteratively sequences through a series of methods and algorithms to attain optimal convergence
- Selects from multiple solvers based on circuit topology to use the best solver for the circuit application
- Offers multiple options for controlling convergence

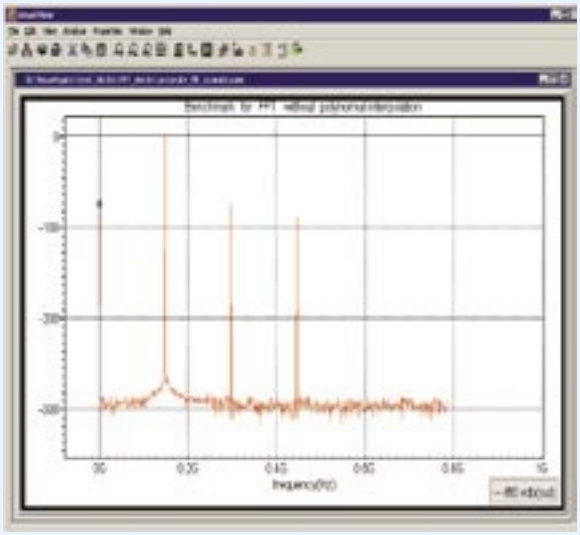
Ease of Adoption: SmartSpice fits your design flow and foundry models

- Supports foundry-supplied SmartSpice and HSPICE™ models
- Supports legacy netlists from HSPICE™, PSPICE™, and Berkeley SPICE
- Seamless integration with Cadence analog environment through OASIS™
- Total integration with Silvaco Custom IC CAD tool flow

Model Development Capabilities

- Core competence in SPICE modeling, data acquisition and model parameter extraction since 1984 with UTMOST™ for the highest accuracy in analog models
- Verilog-A models offer fastest method for implementing OVI standard electric-thermal models, sensor models, and other mixed physical effects
- "C" Interpreter enables modeling engineers to quickly interpret and debug models external to SmartSpice
- SmartSpice is first to deliver Berkeley models with proven BSIM4 solution correcting negative capacitance in original Berkeley implementation
- Silvaco offers accurate and prompt SPICE Modeling Services to extract DC, AC (S-parameters), capacitance, temperature, noise, and SPICE parameters over full temperature and corner models using statistical analysis

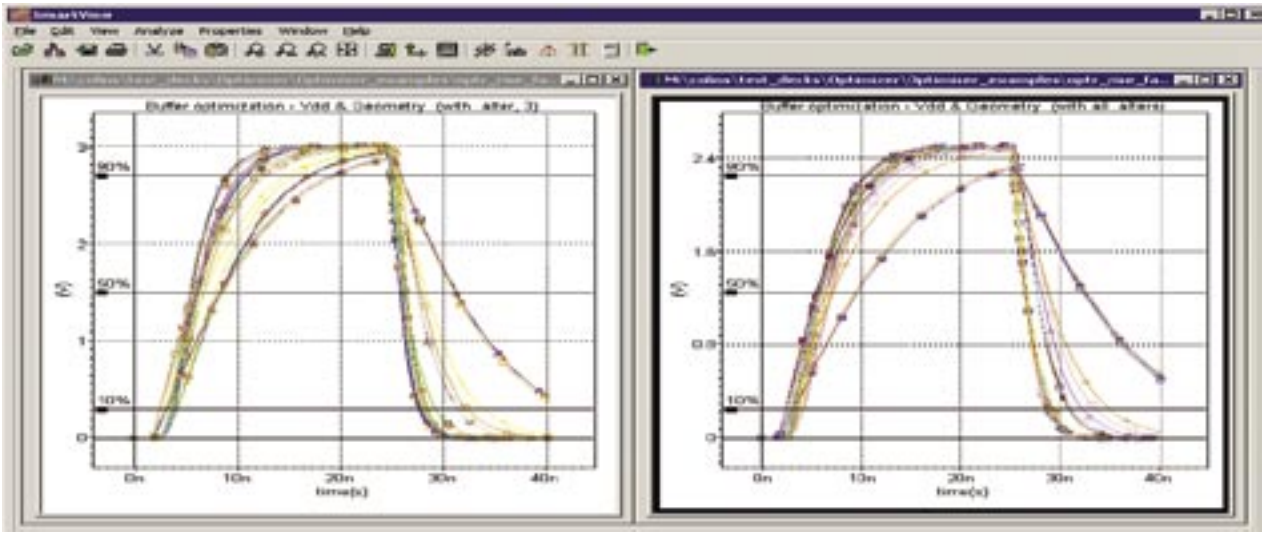




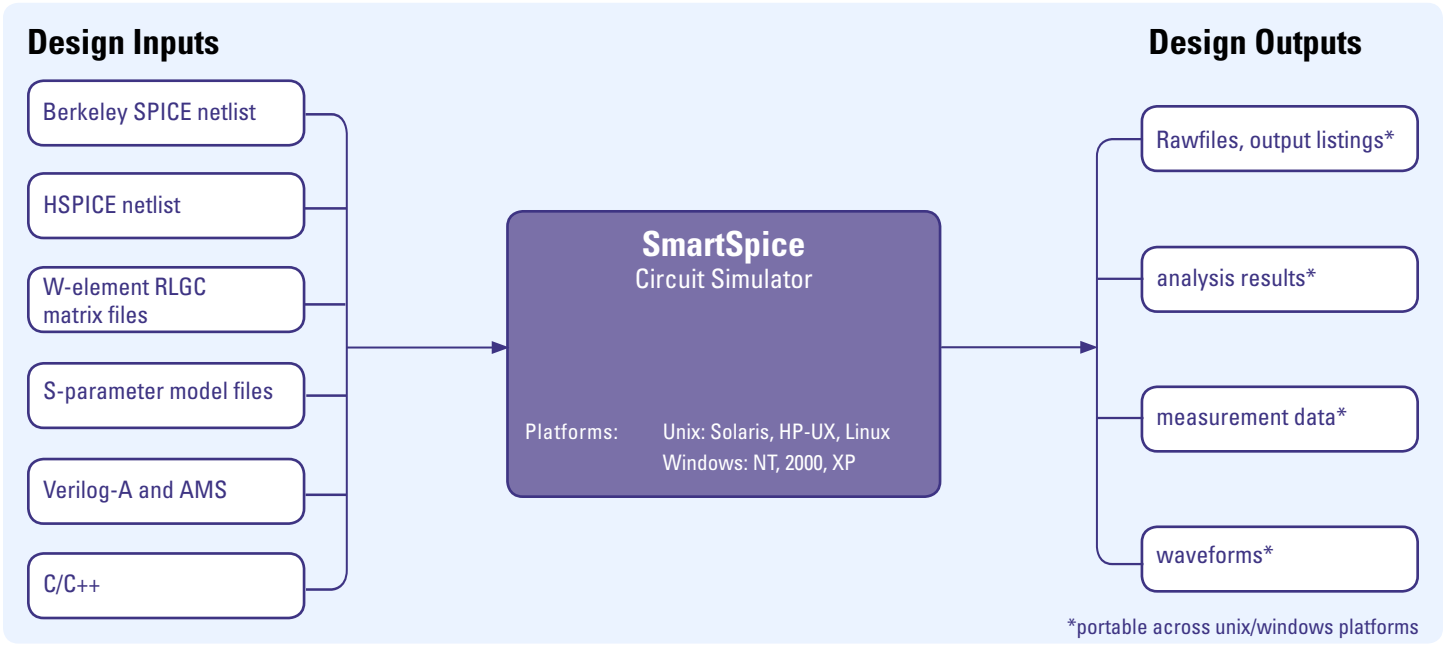
SmartView™: produces annotated plots and graphs of measurements of time, voltage, current, and power for rise time, slope, vector calculator, and eye diagrams from SmartSpice and HSPICE™ simulation results.

Models Available

BJT:	Philips Mextram/MODELLA, HiCUM, VBIC, Quasi-RC, IGBT, QBBJT, Modified Gummel-Poon
MOSFET:	Berkeley (Levels 1, 2, 3); BSIM (1, 3v3,4); Philips MOS (9,11), Hspice Level 28, EKV, HiSIM, HVMOS
TFT:	Amorphous TFT, Polysilicon TFT, Berkeley, Leroux, RPI
SOI:	Berkeley BSIM3SOI PD/DD/FD, STAG, UFS, LETISOI
HBT:	UCSD
MESFET:	Stats, Curtice I & II, TriQuint 1/2/3
JFET:	Berkeley Levels 1, 2
Diode:	Berkeley, Fowler-Nordheim, Philips JUNCAP/Level 500
FRAM:	Ramtron FCAP



Integrated Optimizer iterates device or model parameters to achieve target specifications in the form of DC, AC, transient curves, propagation delay, rise and fall times, power dissipation, etc.



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