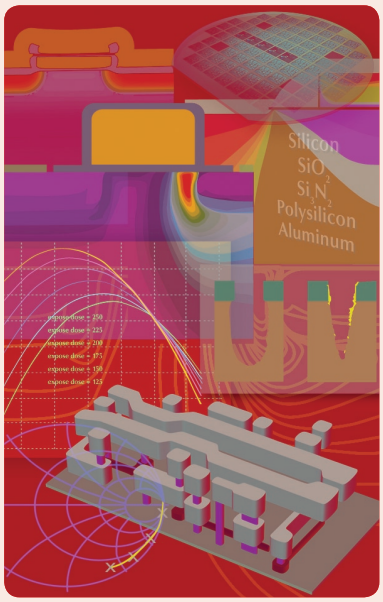
SILVACO

EXACT Interconnect Parasitic Characterization



EXACT™ Interconnect Parasitic Characterization delivers the most accurate interconnect models for nanometer semiconductor processes and generates layout parameter extraction (LPE) rule files for leading full chip extraction tools. EXACT's powerful 3D field solvers support xCalibre™, Calibre xRC™, Diva™, Assura RCX™, and Dracula™ LPE.

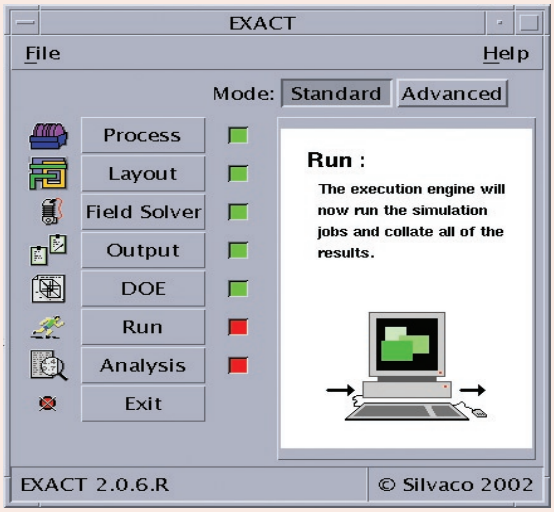
- Powerful 3D solver supports non-planar semiconductor profiles for accurately modeling irregular etch profiles, dual damascene, and low-K dielectrics
- 3D field solver calculates interconnect capacitance models to deliver highest accuracy LPE rule files without compromising extraction performance
- Intuitive and user-friendly graphical interface for process layer description and test structure definition for beginner and experienced process technology developers
- Standard mode of operation handles most conventional processes whereas advanced mode can be used for more complex and non-planar process definition
- Integrated scripting language provides custom LPE rule files for other extraction tools
- Powerful statistical analysis module option available to calculate variations of capacitance using known process margins to account for interconnect process variations

Ease of Use and Adoption

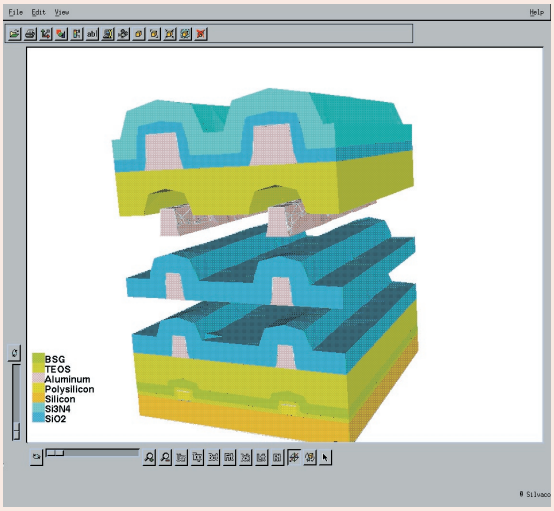
- Easy to use, menu-driven graphical interface for process layer definition and conversion of legacy Raphael™ files
- Easy LPE rule generation with LISA™ scripting language
- Menu-driven parameterized layout generator for test structure and pattern generation
- Flexible architecture for fitting raw parasitic data into a wide range of custom equations for xCalibre™, Calibre xRC™, and Assura-RCX™/Diva™/Dracula™ LPE

Productivity and Versatility

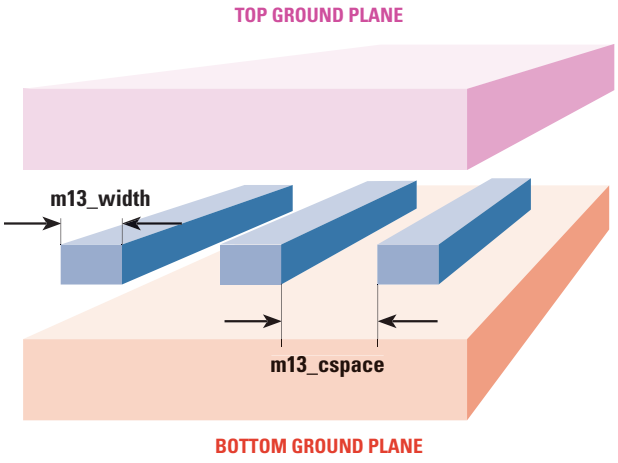
- Batch mode operation allows pipeline submitting of overnight runs
- Advanced mode operation is designed to allow experienced users to have more control over the field solver to address more complex process topology
- Inclusion of process variables in experiments to perform statistical analysis on interconnect capacitance variations
- Easy to understand extracted capacitance tables that facilitate the analysis of effects on interconnect due to various process change or experiment
- Automatic deck generation and submission to 3D field solver

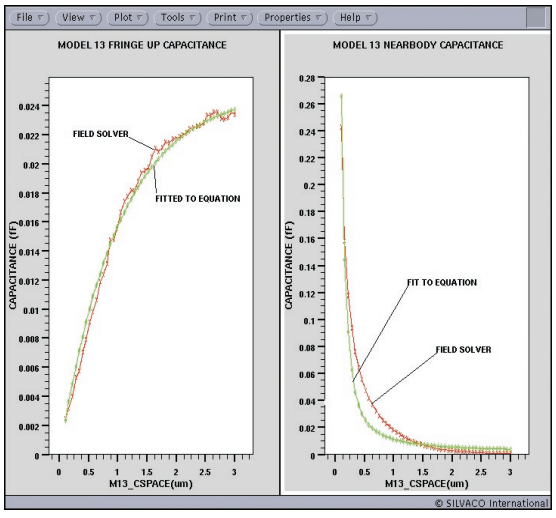


Front-end to EXACT.



Multilevel metal process with conformally deposited, non-planar multiple dielectrics.





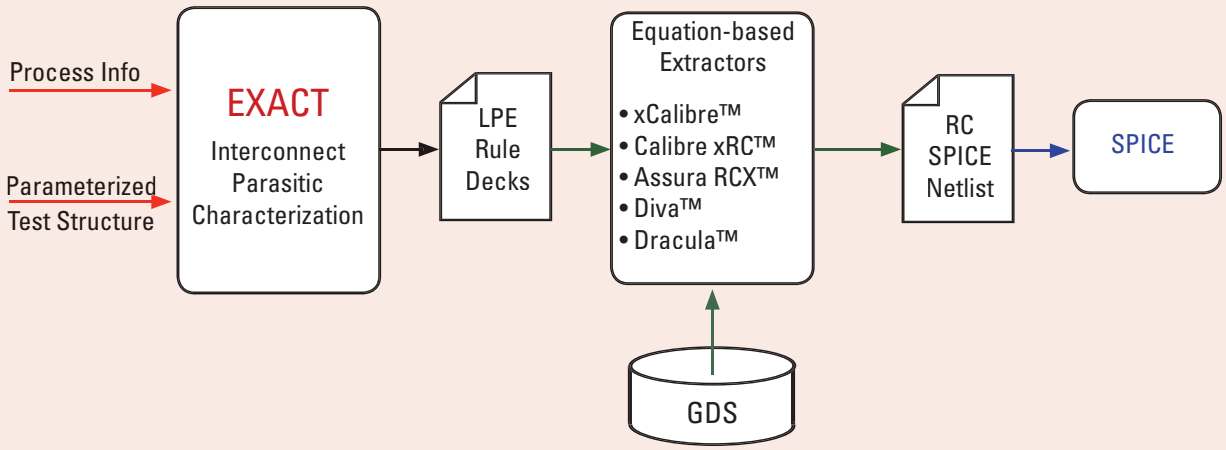
Field solver results and fitted equation for the structure on the left.

Advanced Semiconductor Process Support

Interconnect parasitic capacitance modeling support for

- Planar and non-planar dielectrics
- Low-K dielectric and copper damascene process
- Conformal dielectrics deposition
- Sub-wavelength lithographic effects due to optical proximity correction (OPC)
- Process variations impact on interconnect capacitance
- Statistical analysis and worst-case parasitic analysis by applying known process margins to extracted data
- Powerful 3D solver supports non-planar semiconductor profiles for accurately modeling irregular etch profiles, dual damascene, and low-K dielectrics
- 3D field solver calibrates interconnect capacitance models to deliver highest accuracy LPE rule files without compromising extraction performance
- Built-in Optimizer enables improved fitting and process optimization

EXACT takes process information and produces LPE rule decks.




```
CAPACITANCE INTRINSIC FRINGE metal2
[
        PROPERTY C
        max_caldistance = 5
        max_distance = 3
        C= 0.0
        if (distance() > 0.0) {
              C =0.01001*(1.0 - exp(-1.65*(distance()+0.075)))*length()
        }
        if (distance() <= 0.0) {
        C = 0.0304042* length()
        }
]


CAPACITANCE NEARBODY poly1

[
        PROPERTY C
        max_width = 3
        max_distance = 3
        C=0.932762*length()*pow(0.1,0.0536348)*1.0*(exp((-distance()*1.60124)-2.96352)
           +(0.00677904/pow(distance(),1.3288)))
]
```

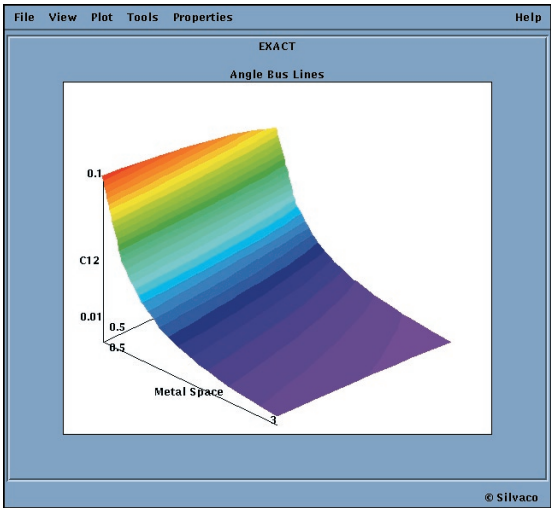
Mentor Graphics xCalibre™/Calibre xRC™ rule file generated by EXACT.

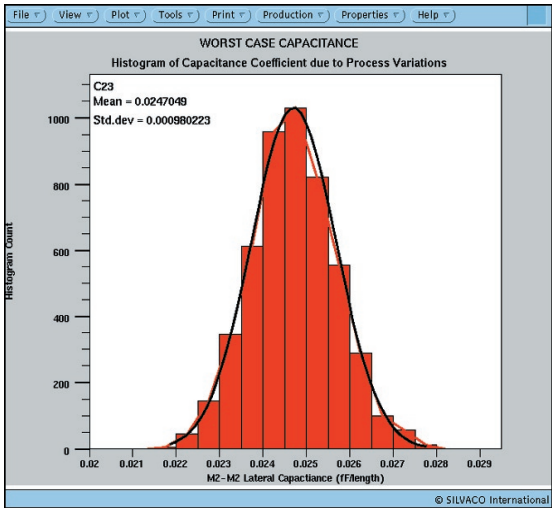
```
;Diva rule file for same layer nearbody capacitance
;Uses OneArray like structure

metal1_metal1_fcap=measureFringe(
metal1
calculate(1*(0.0510802/(pow((s+0.133027),1.30154))))
ML MLlayer_metal1
sep < 3.588
opposite
shielded
diffNet


metal2_metal2_fcap=measureFringe(
metal2
calculate(1*(0.0173255/(pow((s+0.0676441),1.01108))))
ML MLlayer_metal2
sep < 3.588
opposite
shielded
diffNet
```

Cadence Diva™ rule file generated by EXACT.

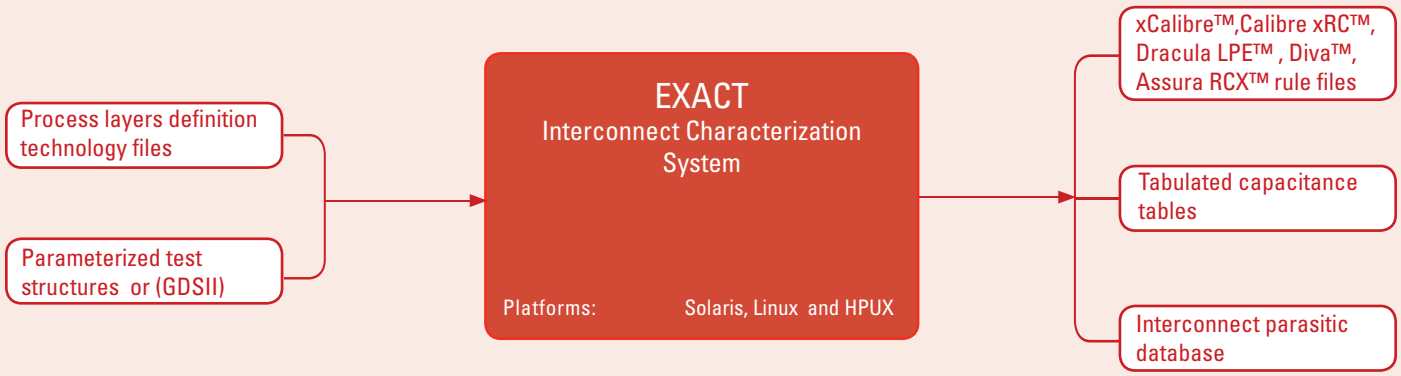




Variation of capacitance coefficient with process variables can be seen graphically (left) or analyzed statistically (right). The histogram shows the expected distribution in lateral capacitance with known margin on metal geometry.

Design Inputs

Design Outputs



SILVACO

USA Headquarters:

Silvaco International
4701 Patrick Henry Drive, Bldg. 2
Santa Clara, CA 95054 USA
Phone: 408-567-1000

Fax: 408-496-6080
sales@silvaco.com
www.silvaco.com

Worldwide:

Japan: jpsales@silvaco.com
Korea: krsales@silvaco.com
Taiwan: twsales@silvaco.com
Singapore: sgsales@silvaco.com
UK: uksales@silvaco.com
France: frsales@silvaco.com
Germany: desales@silvaco.com