The Foundations of the EKV MOS Transistor Charge-Based Model

Christian Enz[1,2], M. Bucher[3], A.-S. Porret[4], J.-M. Sallese[2] and F. Krummenacher[2]

[1] Swiss Center for Electronics and Microtechnology (CSEM), Neuchâtel, Switzerland,
[2] Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland,
[3] National Technical University of Athens, Greece,
[4] Xceive Inc., San Jose, USA.

ABSTRACT

This paper presents the foundations that lead to the EKV MOS transistor compact model. It describes all the basic concepts required to derive the large-signal and small-signal charge-based model that is valid in all modes of inversion, from weak to strong inversion through moderate inversion. The general small-signal model valid in quasi-static and non-quasi-static operation is also presented and all its components are described. It is also shown that the charge-based approach allows to derive the g_m/I_D characteristic that is valid in all modes of inversion.

I. INTRODUCTION

There has been an increasing interest in the recent years for charge-based and surface potential MOST models since they allow to cover a wide range of bias in a continuous way [1], [1], [2], [3], [4]. They also allow to separate the fundamental physical relations existing between the charges and the currents on one hand and the charges and the terminal voltages on the other. This paper presents the foundations of the large-signal and small-signal quasi-static and non-quasi-static EKV charge-based model.

II. BASIC CONCEPTS

A. Device Symmetry

As shown in the cross-section of Fig. 1, the MOST is basically symmetrical with respect to the source and the drain. This feature can be exploited when modelling the device by referring the terminal voltages to the local substrate instead of the source electrode as it is usually done in most Spice compact models. This leads to expressions that are symmetrical with respect to the source and the drain voltage [5].

B. Drain Current

The drain current is given by [6]

$$I_D = \mu_n W \left(-Q_i' \cdot \frac{d\Psi_s}{dx} + U_T \cdot \frac{dQ_i'}{dx} \right)$$
$$= \mu_n W (-Q_i') \cdot \frac{dV_{ch}}{dx}, \tag{1}$$

where μ_n is the *carrier mobility* (assumed to be constant along the channel), W is the *channel width*, Q_i' is the *inversion charge density*, Ψ_s the *surface potential* and $U_T \triangleq kT/q$ the *thermodynamic voltage*. V_{ch} is the *channel voltage*, defined as the quasi-Fermi potential of the minority carrier and representing the disequilibrium introduced
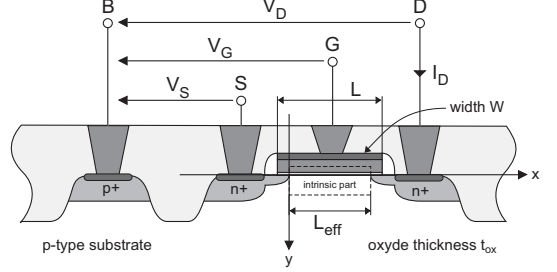

Fig. 1. MOST cross-section.

by non-zero source and drain voltages [5]. V_{ch} is equal to V_S at the source (i.e. for $x = 0$) and V_D at the drain (i.e. for $x = L_{eff}$).

C. Inversion Charge Linearization

The EKV charge model is based on the fundamental relations existing between the charges, the transconductances and the surface potential. The inversion charge density Q_i' is given by [5], [6]

$$Q_i' = C_{ox}' \cdot (V_G - V_{FB} - \Psi_s - \gamma_s \sqrt{\Psi_s}). \tag{2}$$

where $C_{ox}' \triangleq \epsilon_{ox}/t_{ox}$ is the *oxyde capacitance per unit area*, V_{FB} the *Flat-Band voltage* (accounting also for the effective interface charge Q_{ox}') and γ_s is the *substrate factor* defined by [5], [6]

$$\gamma_s \triangleq \frac{\sqrt{2q\epsilon_{si}N_s}}{C_{ox}'}, \tag{3}$$

where N_s is *doping level* in the substrate (assumed to be constant in the channel region), q the elementary charge and ϵ_{si} is the silicon permittivity.

Fig. 2 shows that, at a given gate voltage, Q_i' is almost a linear function of Ψ_s in the inversion region [7]. It can therefore be approximated as

$$Q_i' \cong n_q \cdot C_{ox}' \cdot (\Psi_s - \Psi_{s0}), \tag{4}$$

where Ψ_{s0} is the value of Ψ_s for which $Q_i' = 0$ for a given gate voltage, which depends on V_G according to

$$\Psi_{s0} = V_G - V_{FB} + \gamma_s \cdot \left(\frac{\gamma_s}{2} - \sqrt{\left(\frac{\gamma_s}{2}\right)^2 + V_G - V_{FB}} \right). \tag{5}$$

Factor n_q in (4) is defined as [8], [7], [9]

$$n_q \triangleq \frac{1}{C_{ox}'} \cdot \left. \frac{\partial Q_i'}{\partial \Psi_s} \right|_{V_G} = 1 + \frac{\gamma_s}{2 \cdot \sqrt{\Psi_s}} \tag{6}$$
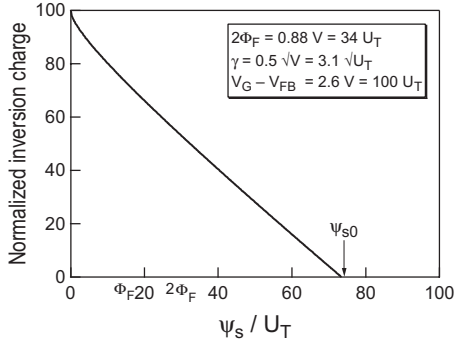
Fig. 2. Inversion charge density Q'_i normalized to $C'_{ox}U_T$ versus the surface potential normalized to U_T.

Fig. 3. Surface potential versus channel voltage.

and where Ψ_s is chosen between $2\Phi_F$ and Ψ_{s0} in order to minimize the approximation error with Φ_F being the *electrons Fermi potential*.

D. Current and Charge Normalization

The above charge linearization allows to write the derivative of the surface potential as [1], [3], [8]

$$\frac{d\Psi_s}{dx} = \frac{1}{n_q C'_{ox}} \cdot \frac{dQ'_i}{dx}, \qquad (7)$$

which can be used in (1) to express the drain current as a function of the inversion charge density [8]

$$i_d \triangleq \frac{I_D}{I_S} = -(2q'_i + 1) \cdot \frac{dq'_i}{d\xi}, \qquad (8)$$

where the drain current and the inversion charge density have been normalized with the *specific current* I_S and the *specific charge density* Q'_S respectively, according to [5], [10], [8], [9]

$$I_S \triangleq 2n_q \beta U_T^2 \quad \text{and} \quad Q'_S \triangleq -2n_q C'_{ox} U_T, \qquad (9)$$

with $\beta \triangleq \mu_n C'_{ox} W/L$. The position x has been normalized to the channel length, $\xi \triangleq x/L_{eff}$, and the voltages are all normalized to U_T, $\psi_s \triangleq \Psi_s/U_T$, $v_g \triangleq V_G/U_T$ and $v_{ch} \triangleq V_{ch}/U_T$.

E. Forward and Reverse Modes

The drain current is obtained by integrating (8) from source ($\xi = 0$) to drain ($\xi = 1$), leading to [5]

$$i_d = i_f - i_r = \int_{q_r}^{q_f} (2q'_i + 1) \cdot dq'_i, \qquad (10)$$

where the symmetry property of the device has been used to split the drain current into a *forward current* $i_f \triangleq I_F/I_S$ and a *reverse current* $i_r \triangleq I_R/I_S$ that depend only on the values of the inversion charge density at the source $q_f \triangleq q'_i(\xi = 0)$ and drain $q_r \triangleq q'_i(\xi = 1)$ respectively

$$i_f = q_f^2 + q_f \quad \text{and} \quad i_r = q_r^2 + q_r. \qquad (11)$$
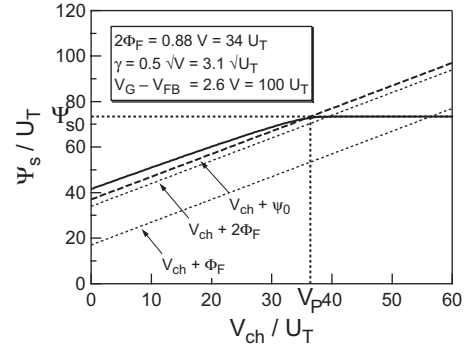
Note that (11) can be inverted to express the forward and reverse charge densities as a function of the forward and reverse currents according to

$$q_f = \frac{2i_f}{\sqrt{4i_f + 1} + 1} \quad \text{and} \quad q_r = \frac{2i_r}{\sqrt{4i_r + 1} + 1}. \qquad (12)$$

The above equations establish a relation between the forward and reverse currents and the forward and reverse charges. The next section will derive a relation between the forward and reverse charges and the voltages.

F. Pinch-off Voltage

As shown in Fig. 3, for a given gate voltage, the surface potential increases with respect to the channel voltage and then saturates to Ψ_{s0} in weak inversion. In strong inversion, Ψ_s can therefore be approximated by a linear function of the channel voltage according to

$$\Psi_s \cong V_{ch} + \Psi_0, \qquad (13)$$

with $\Psi_0 \triangleq 2\Phi_F + m \cdot U_T$, where m is a parameter which is typically chosen between 2 and 4 in order to minimize the approximation error. The *pinch-off voltage* V_P is then defined as the channel voltage for which the inversion charge becomes zero under strong inversion assumption (i.e. assuming there is no moderate nor weak inversion) [5]. By definition of Ψ_{s0}, it corresponds in Fig. 3 to the intersection between the approximation given by (13) and Ψ_{s0}

$$\Psi_{s0} \triangleq V_P + \Psi_0. \qquad (14)$$

Introducing (14) into (2) and setting $Q'_i = 0$, leads to

$$V_G - V_{FB} = V_P + \Psi_0 + \gamma_s \cdot \sqrt{V_P + \Psi_0}, \qquad (15)$$

which can be inverted to express V_P as a function of V_G [5],

$$V_P = V_{GT} - \gamma_s \cdot \left[\sqrt{V_{GT} + \left(\sqrt{\Psi_0} + \frac{\gamma_s}{2}\right)^2} - \left(\sqrt{\Psi_0} + \frac{\gamma_s}{2}\right) \right], \qquad (16)$$

where $V_{GT} \triangleq V_G - V_{TO}$ is the *overdrive voltage* and $V_{TO} \triangleq V_{FB} + \Psi_0 + \gamma_s \cdot \sqrt{\Psi_0}$ is the *threshold voltage*.
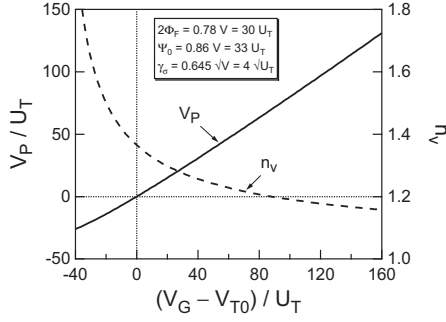
Fig. 4. Pinch-off voltage versus gate voltage.

Fig. 5. Normalized g_m/I_D function measured for several different processes.

As shown in Fig. 4, the pinch-off voltage is almost a linear function of the gate voltage and can therefore be approximated by [5]

$$V_P \cong \frac{V_G - V_{TO}}{n_v},\qquad(17)$$

where n_v is defined as [5], [9]

$$n_v \triangleq \frac{dV_G}{dV_P} = 1 + \frac{\gamma_s}{2 \cdot \sqrt{\Psi_0 + V_P}}\qquad(18)$$

and is a function of the pinch-off voltage and therefore also of the gate voltage as illustrated in Fig. 4.

It can be shown that there is a general relation between the inversion charge density, the pinch-off voltage and the channel voltage which is valid all along the channel [10], [8], [9]

$$v_p - v_{ch}(\xi) = \ln(q_i'(\xi)) + 2q_i'(\xi).\qquad(19)$$

Eqn. 19 is of course valid at the source (where $q_i' = q_f$) and the drain (where $q_i' = q_r$) leading to

$$v_p - v_s = \ln(q_f) + 2q_f, \quad v_p - v_d = \ln(q_r) + 2q_r.\qquad(20)$$

A relation between the voltages and the currents is obtained by replacing q_f (q_r) by (12) in (20) resulting in [2]

$$v_p - v_s = \ln(\sqrt{i_f + \tfrac{1}{4}} - \tfrac{1}{2}) + \sqrt{4i_f + 1} - 1,\qquad(21a)$$

$$v_p - v_d = \ln(\sqrt{i_r + \tfrac{1}{4}} - \tfrac{1}{2}) + \sqrt{4i_r + 1} - 1.\qquad(21b)$$

Unfortunately (21a) and (21b) cannot be inverted analytically to express the current as a function of the terminal voltages, as it is required by a circuit simulator. Nevertheless it can either be inverted numerically with just a few iterations or approximated by an analytical function within the range of interest with a negligible error.

III. SMALL-SIGNAL MODEL

A. Transconductances

By definition, the *source* and *drain transconductances* g_{ms} and g_{md} are proportional to the charges at the source and drain q_f and q_r respectively. Replacing q_f and q_r by (12) results in [2], [3]

$$g_{ms} = Y_0 \cdot q_f = Y_0 \cdot \frac{2i_f}{\sqrt{4i_f + 1} + 1},\qquad(22a)$$

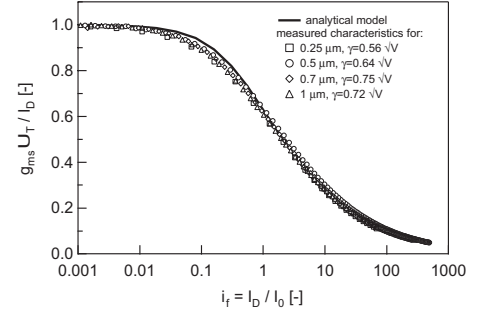$$g_{md} = Y_0 \cdot q_r = Y_0 \cdot \frac{2i_r}{\sqrt{4i_r + 1} + 1},\qquad(22b)$$

where $Y_0 \triangleq I_S/U_T$. Eqn. (22a) can then be used to derive the g_m/I_D characteristic [2], [3]

$$\frac{g_{ms} \cdot U_T}{I_F} = \frac{g_{ms}}{i_f \cdot Y_0} = \frac{2}{\sqrt{4i_f + 1} + 1},\qquad(23)$$

which is often used in analog IC design to set the correct operating point (i.e. inversion factor $IC \triangleq i_f$) in saturation corresponding to a desired transconductance at a given current. It is plotted in Fig. 5 together with data measured on several different processes.

Fig. 6. MOST intrinsic small-signal schematic.

B. HF Small-Signal Model

The general small-signal model of the intrinsic MOST, valid in Non-Quasi-Static (NQS) mode of operation [10], is presented in Fig. 6 together with the definitions of the voltage controlled current sources (VCCS) [11]. The *gate transadmittance* Y_m depends on the *source* and *drain transadmittances* Y_{ms} and Y_{md} according to [10], [11]

$$Y_m = \frac{1}{n_v} \cdot (Y_{ms} - Y_{md}),\qquad(24)$$

with $Y_{ms} \cong g_{ms} \cdot \xi_m$ and $Y_{md} \cong g_{md} \cdot \xi_m$ [11], where ξ_m is a bias independent function that accounts for the NQS effects and therefore for the frequency dependence using a frequency normalized to $\omega_{qs} \triangleq 1/\tau_{qs}$ which corresponds to the limit between quasi-static (QS) and non-quasi-static (NQS) operation [11]. ξ_m is plotted versus $\omega\tau_{qs}$ in Fig. 7 a) (black line) and is compared to measurements made at different bias (grey lines) [11].

The admittance Y_{gsi} can also be decomposed into a product [11], [12]

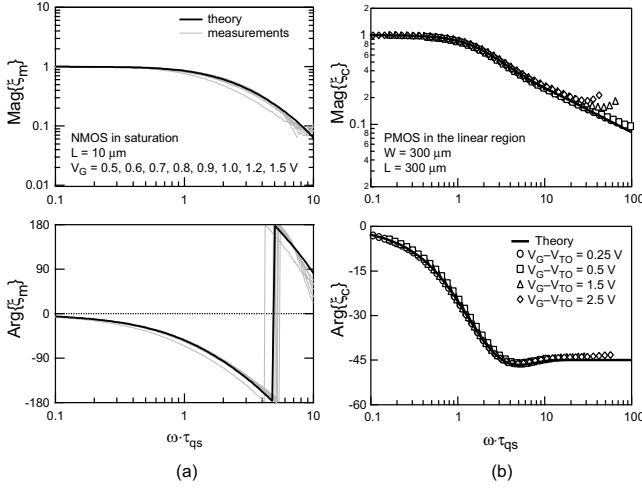$$Y_{gsi} = j\omega C_{ox} \cdot c_c \cdot \xi_c,\qquad(25)$$

Fig. 7. ξ_m (a) and ξ_c (b) versus frequency.

where $C_{ox} \triangleq WLC'_{ox}$ is the total gate oxide capacitance, c_c is a normalized capacitance that depends only on the bias conditions through q_f and q_r and ξ_c is a transfer function that accounts for the NQS effects. A general expression of ξ_c valid in all regions of operation is presented in [11], [12]. The NQS function ξ_c is plotted versus $\omega\tau_{qs}$ in Fig. 7 b). It clearly shows the -45 asymptote of the phase reached for $\omega\tau_{qs} \gg 1$, which is characteristic of NQS effects. The symbols correspond to the data measured on a PMOS device biased in the linear region ($V_{DS} = 0$) for several gate voltages. Note that in strong inversion and in saturation (i.e. for $q_f \gg 1$ and $q_r \ll 1$), the normalized capacitance c_c tends to 2/3, whereas in the linear region (i.e. for $q_f = q_r \gg 1$) it reduces to 1/2. In weak inversion (i.e. for both $q_f \ll 1$ and $q_r \ll 1$), c_c reduces to q_f, which corresponds to a diffusion capacitance since q_f is proportional to the current in weak inversion.

Admittance Y_{gbi} is given by [11]

$$Y_{gbi} = \frac{n_v - 1}{n_v} \cdot (j\omega C_{ox} - Y_{gsi} - Y_{gdi}), \qquad (26)$$

where Y_{gdi} is simply obtained from Y_{gsi} in (25), by exploiting the source and drain symmetry (i.e. permuting q_f with q_r in the expressions of c_c and ξ_c given in [11], [12]). Finally, Y_{bsi} and Y_{bdi} are obtained from the following fundamental relations [5], [11]

$$Y_{bsi} = (n_v - 1) \cdot Y_{gsi}, \quad Y_{bdi} = (n_v - 1) \cdot Y_{gdi}. \qquad (27)$$

The above formulation is very compact and covers a wide range of bias and frequency. Note that for $\omega \ll \omega_{qs}$, the NQS functions ξ_m and ξ_c simplify to their QS approximations $\xi_m \cong 1 - j\omega\tau_{qs}$ and $\xi_c \cong 1$, meaning that the admittances in Fig. 6 reduce to capacitances.

IV. CONCLUSION

The EKV MOST charge-based model is based on fundamental physical considerations and relations between the current, the charges, the voltages and the small-signal parameters that are valid in all modes of inversion. The model derivation starts with exploiting the device symmetry and the linearization of the inversion charge density to express the forward and reverse normalized currents as a function of the forward and reverse normalized charges. It then introduces the pinch-off voltage to account for the substrate effect and refer the effect of the gate voltage to the channel. This allows to derive exact relations between the control voltages and the forward and reverse currents that are valid in all modes of inversion.

The small-signal model is based on a simple equivalent schematic which is valid in QS and NQS modes of operation. By using a proper bias and frequency normalization, only two basic functions are required to describe all the components of the small-signal schematic. One is used for the transadmittances and the other for the admittances. The fundamental relations existing between the transconductances and the charges also allow to derive a normalized g_m/I_D function valid from weak to strong inversion.

All these fundamental relations can also be used to extend the basic intrinsic long-channel model presented herein in order to include important effects related to the reduction of the device geometry [4], [7], [13].

REFERENCES

[1] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An Explicit Physical Model for Long-Channel MOS Transistor Including Small-Signal Parameters," *Solid-State Elec.*, vol. 38, no. 11, pp. 1945–1952, 1995.

[2] M. Bucher, C. Lallement, C. Enz, F. Theodoloz, and F. Krummenacher, "Scalable g_m/I Based MOSFET Model," *Proc. of the Int. Semiconductor Device Res. Symp.*, Dec. 1997.

[3] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS Transistor Model for Analog Circuit Design," *IEEE J. of Solid-State Circ.*, vol. 33, no. 10, pp. 1510–1519, Oct. 1998.

[4] M. Bucher, J.-M. Sallese, C. Lallement, W. Grabinski, C. C. Enz, and F. Krummenacher, "Extended Charges Modeling for Deep Submicron CMOS," *Proc. of the Int. Semiconductor Device Res. Symp.*, pp. 397–400, Dec. 1999.

[5] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications," *Analog Integrated Circuits and Signal Processing Journal*, vol. 8, pp. 83–114, July 1995.

[6] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, Mc-Graw-Hill, 2nd edition, 1999.

[7] J.-M. Sallese, M. Bucher, and C. Lallement, "Improved Analytical Modeling of Polysilicon Depletion in MOSFETs for Circuit Simulation," *Solid-State Elec.*, vol. 44, no. 6, pp. 905–912, June 2000.

[8] J.-M. Sallese, W. Grabinski, A.-S. Porret, M. Bucher, C. Lallement, F. Krummenacher, C. Enz, and P. Fazan, "Advancements in dc and RF MOSFET Modeling with The EPFL-EKV Charge-Based Model," *Proc. of the 8th Int. Conf. on Mixed-Signal Design*, June 2001.

[9] M. Bucher, *Analytical MOS Transistor Modelling for Analog Circuit Simulation*, PhD Thesis No. 2114, EPFL, 1999.

[10] J.-M. Sallese and A.-S. Porret, "A Novel Approach to Charge Based Non Quasi Static Model of the MOS Transistor Valid in All Modes of Operation," *Solid-State Elec.*, vol. 44, no. 6, pp. 887–894, June 2000.

[11] A.-S. Porret, J.-M. Sallese, and C. C. Enz, "A Compact Non Quasi-Static Extension of a Charge-Based MOS Model," *IEEE Trans. on Elec. Dev.*, vol. 48, no. 8, pp. 1647–1654, Aug. 2001.

[12] C. C. Enz, "A MOS Transistor Model for RF IC Design Valid in All Regions of Operation," *IEEE Trans. on Microwave Theory and Techniques*, 2002, accepted for publication.

[13] M. Bucher, C. Enz, F. Krummenacher, J.-M. Sallese, C. Lallement, and A.-S. Porret, "The EKV 3.0 Compact MOS Transistor Model: Accounting for Deep-Submicron Aspects," *WCM-MCM*, April 2002, in this issue.