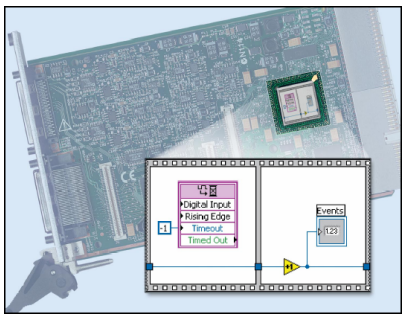
LabVIEW FPGA Module



LabVIEW FPGA Module

- Download LabVIEW graphical code to NI Reconfigurable I/O hardware
- Draw logic to implement advanced timing and triggering, on-board decision making, and custom digital I/O
- Execute tasks deterministically and simultaneously in hardware
- Requires no knowledge of VHDL or FPGA design tools

Operating System
Windows 2000/XP

Required Software
LabVIEW Full or Professional Development System, current version

Recommended Software
LabVIEW Real-Time Module

Supported Hardware
PXI-7831R Reconfigurable I/O

Overview

National Instruments LabVIEW and LabVIEW FPGA Module deliver graphical development for Field-Programmable Gate Array (FPGA) chips on NI Reconfigurable I/O hardware. With the LabVIEW FPGA Module, you develop FPGA VIs on a host computer running Windows, then LabVIEW compiles and implements the code in hardware. Create embedded FPGA VIs that combine direct access to I/O with user-defined LabVIEW logic to define custom hardware for rapid prototyping, device simulation, custom communication protocols, and closed-loop control.

Graphical Development

The LabVIEW FPGA Module extends the LabVIEW development environment to compile and download VIs to NI Reconfigurable I/O hardware. When targeted to the FPGA device, LabVIEW displays a customized palette that includes operations that can be implemented in hardware. The FPGA hardware palette includes functions such as for loops, while loops, case statements, sequence structures, integer math functions, comparison and boolean operators, array and cluster tools, data manipulation, occurrences, analog and digital I/O, and timing. The analog and digital input/output nodes access signals directly from the connectors of the Reconfigurable I/O hardware. The timing functions take advantage of the on-board clock, achieving timing resolution of 25 nanoseconds for the PXI-7831R.

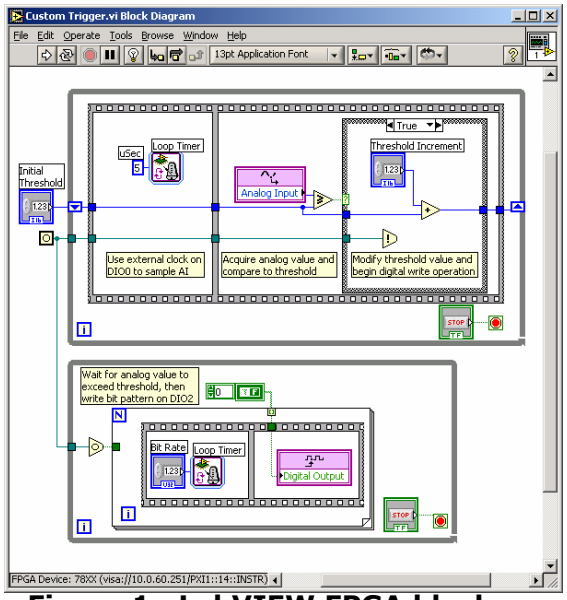


Figure 1. LabVIEW FPGA block diagram of a custom trigger

Use a combination of LabVIEW functions to define logic and embed intelligence in your I/O. Figure 1 is an example of a custom trigger application developed in LabVIEW and downloaded to a PXI-7831R Reconfigurable I/O device. The upper while loop samples an analog input signal at a rate specified by an external clock. If the value of the signal exceeds the threshold value, the VI calculates a new threshold value and uses an occurrence to begin executing the lower while loop. The lower while loop writes a predefined bit pattern to one of the digital lines on the board and then waits for the next trigger. By defining the logic in LabVIEW and downloading the code to the on-board FPGA, the PXI-7831R performs as a custom trigger board. This board can also be combined with additional PXI modules to trigger complementary acquisitions and signal generations.

Parallel Execution

The inherent parallelism of LabVIEW is realized in hardware as true simultaneous execution. The compiled code is implemented in hardware by configuring logic cells in the FPGA. Your embedded VI does not need access to a processor to execute. Independent sections of code, such as parallel while loops, are implemented in independent sections of the FPGA. After the chip is configured, data is clocked through the device at a rate specified by the on-board clock, executing independent areas of the chip simultaneously. In Figure 1, the parallelism of LabVIEW FPGA and Reconfigurable I/O enables the analog and digital loops to execute simultaneously without competing for execution time from the host processor.

Debugging Tools

Depending on the complexity of your code and the specifications of your development system, the compile time for an FPGA VI can range from minutes to several hours. Therefore, the LabVIEW FPGA Module includes a device emulator, so you can verify the logic of your design before initiating the compile process. While targeted to the FPGA emulator, LabVIEW accesses real I/O from the device as the VI logic executes on the Windows machine. In this mode, you can use the same debugging tools available in LabVIEW for Windows, such as execution highlighting, probes, and breakpoints.

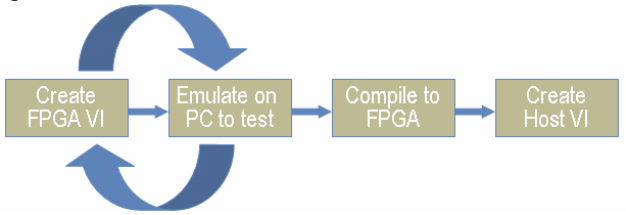


Figure 2. Application development flow for systems using the LabVIEW

User Interface

The embedded FPGA VI can execute autonomously or be combined with LabVIEW Real-Time or LabVIEW for Windows to integrate floating point calculations, networking, file I/O, and user interface operations. LabVIEW Real-Time provides a deterministic execution system for functions performed outside of the FPGA, such as floating-point arithmetic including FFTs, PID calculations, and custom control algorithms. Relevant data can be stored to a LabVIEW Real-Time system or transferred to the LabVIEW for Windows for off-line analysis, remote data logging, or user interface display.

Each control and indicator of the embedded VI is implemented as a register in the FPGA. From a LabVIEW Real-Time or LabVIEW for Windows application, you can access the data in these controls and indicators using programming similar to VI Server. In your host application, you create a reference to your embedded VI, interact with the data in the controls and indicators, and then close your session.

System Requirements

- Windows 2000/XP
- 1 GHz Pentium processor
- 512 MB RAM
- 800 X 600 screen resolution
- TCP drivers installed

Ordering Information

LabVIEW FPGA Module †	778694-03

† Requires current version of LabVIEW Full or Professional Development System